

AST - 10214662.wsp.1

File View Edit Insert Window Help

Active

- ↳ L1: (24668) insulat\$3 adj layer and gate adj electrode and substrate
- ↳ L2: (62831) (bit adj line) or bitline
- ↳ L3: (2562) ((bit adj line) or bitline) with cover\$3
- ↳ L4: (21) 3 with isolation adj layer
- ↳ L5: (474263) 4 and contact plug
- ↳ L6: (10) 4 and contact adj plug
- ↳ L7: (4) 6 and buried

Failed

Saved

- ↳ (8760) (257/295-313,903-908) CCLS.
- ↳ (76340) DRAM
- ↳ (3289) ((257/295-313,903-908),CCLS.) and DRAM
- ↳ (21217) DRAM and insulat\$3
- ↳ (6931) (DRAM and insulat\$3) and gate adj electrode
- ↳ (402) (DRAM and insulat\$3) and gate adj electrode) and isolat\$3 adj layer
- ↳ (74) (((DRAM and insulat\$3) and gate adj electrode) and isolat\$3 adj layer) and contact adj plug
- ↳ (6) (((DRAM and insulat\$3) and gate adj electrode) and isolat\$3 adj layer) and buried adj contact

Favorites

Document ID Issue Date Pages Title Current Cur Re Inventor S C P R I

1	r r US 20020149977 A1	20021017	9	Semiconductor memory	365/200	Oh, Jae-Hee	P	R	R	R	R
2	r r US 6620685 B2	20030916	8	Method for fabricating of 438/257	438/	Oh, Jae-Hee	P	R	E	R	R
3	r r US 6326295 B1	20011204	14	Method and structure for 438/622	257/	Figura, Thomas A.	P	R	R	R	R
4	r r US 6225208 B1	20010501	11	Method and structure for 438/622	257/	Figura, Thomas A.	P	R	R	R	R

L Number	#hits	Search Text	DB	Time stamp
1	24668	insulat\$3 adj layer and gate adj electrode and substrate	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/05 09:25
2	62831	((bit adj line) or bitline)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/05 09:26
3	2562	((bit adj line) or bitline) with cover\$3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/05 09:26
4	21	(((bit adj line) or bitline) with cover\$3) with isolation adj layer	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/05 09:26
5	474263	(((bit adj line) or bitline) with cover\$3) with isolation adj layer and contact plug	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/05 09:27
6	10	(((bit adj line) or bitline) with cover\$3) with isolation adj layer and contact adj plug	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/05 09:27
7	4	((((bit adj line) or bitline) with cover\$3) with isolation adj layer and contact adj plug) and buried	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/05 09:27
-	8760	(257/295-313,903-908).CCLS.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/04 16:13
-	76340	DRAM	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/04 16:13
-	3289	((257/295-313,903-908) CCLS.) and DRAM	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/04 16:13
-	21217	DRAM and insulat\$3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/05 09:24
-	6931	(DRAM and insulat\$3) and gate adj electrode	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/04 16:15

-	402	((DRAM and insulat\$3) and gate adj electrode) and isolat\$3 adj layer	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/04 16:16
-	74	((((DRAM and insulat\$3) and gate adj electrode) and isolat\$3 adj layer) and contact adj plug	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/04 16:16
-	6	((((DRAM and insulat\$3) and gate adj electrode) and isolat\$3 adj layer) and buried adj contact adj plug	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/04 16:16